Status Report LSS

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WaLBerla on Juropa and Jugene

Status Report Juropa and Jugene

- No special requirements
- Weak scaling experiments of up to 130000 cores on Jugene
- Variable length arrays in WaLBerla

![Graph showing performance metrics](image)

- **MFLUPS**
  - SoA VLA
  - SoA Original

- **Domain Size per Core**
  - Values range from 50 to 150

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WaLBerla Core

Features

- Patch hierarchy
- Parallelization
- Support for GPUs and heterogeneous simulations
- Simple static load balancing
- Lid driven cavity
WaLBerla Core Features

Patch Hierarchy
WaLBerla Core Features

Patch Hierarchy

<table>
<thead>
<tr>
<th>Block</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Rank</td>
</tr>
<tr>
<td>• Grid Data</td>
</tr>
<tr>
<td>• Functionality</td>
</tr>
</tbody>
</table>
WaLBerla Core Features

Block
- Rank
- Grid Data
- Functionality

Patch Hierarchy

Patch
- Blocks
- Adaptive Refinement
- Hierarchical
WaLBerla Core Features

- Patch Hierarchy
  - Block
    - Rank
    - Grid Data
    - Functionality
  - Parallelization
    - Block Based
    - Dynamic
    - Generic
  - Patch
    - Blocks
    - Adaptive Refinement
    - Hierarchical
**WaLBerla Core Features**

**Manage Functionalities**
- Functionality: SRT, MRT, GPU, CPU, data layouts, etc.
- Idea
  - Give functions and objects meta information
  - Depending on meta information functionality is selected

**Meta Information**

<table>
<thead>
<tr>
<th>ID Type</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>fs</td>
<td>Fixed for whole simulation</td>
</tr>
<tr>
<td>hs</td>
<td>Fixed per process</td>
</tr>
<tr>
<td>bs</td>
<td>Variable per process</td>
</tr>
</tbody>
</table>
WaLBerla Core Features

Functionality fs
(Srt-LBM)

Process I
Hardware: hsCPU

Process II
Hardware: hsGPU
WaLBerla Core Features

Process I

Hardware: hsCPU
FieldData:
Velocity: Layout zyxf
Density: Layout zyx
PDF: Layout fzyx

Functionality fs
(Srt-LBM)

Process II

Hardware: hsGPU
FieldData:
Velocity(CPU + GPU): Layout zyxf
Density(CPU + GPU): Layout zyx
PDF Buffers(CPU + GPU)
PDF(GPU): Layout zyxf
WaLBerla Core Features

Functionality fs (Srt-LBM)

Process I

Hardware: hsCPU

FieldData:
Velocity: Layout zyxf
Density: Layout zyx
PDF: Layout fzyx

Generic Parallelization

MPI Buffers

Process II

Hardware: hsGPU

FieldData:
Velocity(CPU + GPU): Layout zyxf
Density(CPU + GPU): Layout zyx
PDF Buffers(CPU + GPU)
PDF(GPU): Layout zyx

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Walberla Core Features

Process I

Hardware: hsCPU

FieldData:
- Velocity: Layout zyx
- Density: Layout zyx
- PDF: Layout fzyx

Copy Functions:
- copyFromBuf(fs, hsCPU, bs)
- copyToBuf(fs, hsCPU, bs)

MPI Buffers

Process II

Hardware: hsGPU

FieldData:
- Velocity(CPU + GPU): Layout zyx
- Density(CPU + GPU): Layout zyx
- PDF Buffers(CPU + GPU)
- PDF(GPU): Layout zyx

Functionality fs (Srt-LBM)
Results: Hardware

TinyGPU Cluster

- 8 Nodes
- Dual-Socket Nehalem X5550 (8 Cores Node)
- 24 GB RAM (DDR3-1333)
- 2 NVIDIA Tesla M1060 passive cooling
- (DDR) Infiniband
Results: Node Performance on Woody

Node Performance Woody

100^3

Performance fzyx
Performance zyxzf

MFLUPS

Number of Blocks

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Results: Node Performance on Woody

Node Runtime

100^3, fzyx

- **Timeloop**
- **PDF Sweep**
- **Communication**
- **Timeloop - PDF Sweep**

Time in [s] vs. Number of Blocks
Results: Node Performance on TinyGPU

Node Performance TinyGPU

100^3

MFLUPS

Number of Blocks

1 10 100 1000

Double fzyx

Double zyx

Double zyx

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Results: Node Performance on TinyGPU

Node Performance TinyGPU

100^3

MFLUPS

Number of Blocks

Float fzyx
Float zyxf
Results: Node Performance GPU

Node Performance GPU
100^3

MFLUPS

Number of Blocks

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Results: Scaling Performance on TinyGPU

Weak Scaling TinyGPU
100^3

- Scaling GPU Double
- Scaling GPU Float
- Linear Scaling GPU Float
- Scaling CPU Double zyx
- Scaling CPU Float zyx

MFLUPS

Number of Nodes
Results: Heterogeneous Performance on TinyGPU

Simulation Setup for one Node
- 2 x GPUs + 6 x CPUs
- GPU : 9 x Blocks x 50³
- CPU Core: 1 x Block x 50³

Performance Results

<table>
<thead>
<tr>
<th>Configuration</th>
<th>MFLUPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 x CPU Cores</td>
<td>62</td>
</tr>
<tr>
<td>8 x CPU Cores</td>
<td>82</td>
</tr>
<tr>
<td>1 x GPU</td>
<td>90</td>
</tr>
<tr>
<td>2 x GPUs</td>
<td>178</td>
</tr>
<tr>
<td>2 x GPUs + 6 x CPU Cores</td>
<td>229</td>
</tr>
<tr>
<td>2 x GPUs (Two Blocks)</td>
<td>234</td>
</tr>
</tbody>
</table>

- Using CPUs + GPUs results in a speed up of 51 MFLUPS
- But using several blocks on the GPUs results in a decrease of 56 MFLUPS
Outlook

Tasks for Q1 - Q3

- Optimization of
  - LBM kernels
  - Data exchange on GPUs

- Load balancing
- Porting of applications